19-3641; Rev 0; 4/05

# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers



## General Description

The MAX9234/MAX9236/MAX9238 deserialize three LVDS serial-data inputs into 21 single-ended LVCMOS/LVTTL outputs. A parallel-rate LVDS clock received with the LVDS data streams provides timing for deserialization. The outputs have a separate supply, allowing 1.8V to 5V output logic levels. All these devices are hot-swappable and allow "on-the-fly" frequency programming.

The MAX9234/MAX9236/MAX9238 feature DC balance, which allows isolation between a serializer and deserializer using AC-coupling. Each deserializer decodes data transmitted by one of the MAX9209/MAX9211/MAX9213/MAX9215 serializers.

The MAX9234 has a rising-edge output strobe. The MAX9236/MAX9238 have a falling-edge output strobe. The MAX9234/MAX9236/MAX9238 operate in DC-balanced mode only.

The MAX9234/MAX9236 operate with a parallel input clock of 8MHz to 34MHz, while the MAX9238 operates from 16MHz to 66MHz. The transition time of the single-ended outputs is increased on the low-frequency version parts (MAX9234/MAX9236) for reduced EMI. The LVDS inputs meet ISO 10605 ESD specification, ±25kV for Air Discharge and ±8kV Contact Discharge.

The MAX9234/MAX9236/MAX9238 are available in 48-pin TSSOP packages and operate over the -40°C to +85°C temperature range.

## Applications

Automotive Navigation Systems

Automotive DVD Entertainment Systems

Digital Copiers

Laser Printers

## Features

- **DC Balance Allows AC-Coupling for Wider-Input Common-Mode Voltage Range**
- **On-the-Fly Frequency Programming**
- **Operating Frequency Range**
  **8MHz to 34MHz (MAX9234/MAX9236)**
  **16MHz to 66MHz (MAX9238)**
- **Falling-Edge Output Strobe (MAX9236/MAX9238)**
- **Slower Output Transitions for Reduced EMI (MAX9234/MAX9236)**
- **High-Impedance Outputs when $\overline{PWRDWN}$ Is Low Allow Output Busing**
- **5V-Tolerant $\overline{PWRDWN}$ Input**
- **PLL Requires No External Components**
- **Up to 1.386Gbps Throughput**
- **Separate Output Supply Pins Allow Interface to 1.8V, 2.5V, 3.3V, and 5V Logic**
- **LVDS Inputs Meet ISO 10605 ESD Requirements**
- **LVDS Inputs Conform to ANSI TIA/EIA-644 LVDS Standard**
- **Low-Profile, 48-Lead TSSOP Package**
- **+3.3V Main Power Supply**
- **-40°C to +85°C Operating Temperature Range**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX9234**EUM | -40°C to +85°C | 48 TSSOP |
| **MAX9236**EUM | -40°C to +85°C | 48 TSSOP |
| **MAX9238**EUM | -40°C to +85°C | 48 TSSOP |

***Functional Diagram and Pin Configuration appear at end of data sheet.***

# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND .....-0.5V to +4.0V
$V_{CCO}$ to GND .....-0.5V to +6.0V
RxIN_, RxCLK IN_ to GND .....-0.5V to +4.0V
$\overline{PWRDWN}$ to GND .....-0.5V to 6.0V
RxOUT_, RxCLK OUT to GND .....-0.5V to ($V_{CCO}$ + 0.5V)
Continuous Power Dissipation ($T_A$ = +70°C)
48-Pin TSSOP (derate 16mW/°C above +70°C) ..... 1282mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C

ESD Protection
Human Body Model ($R_D$ = 1.5kΩ, $C_S$ = 100pF)
All Pins to GND .....±5kV
ISO 10605 ($R_D$ = 2kΩ, $C_S$ = 330pF)
Contact Discharge (RxIN_, RxCLK IN_) to GND .....±8kV
Air Discharge (RxIN_, RxCLK IN_) to GND .....±25kV
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +3.0V to +3.6V, $V_{CCO}$ = +3.0V to +5.5V, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = $V_{CCO}$ = +3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.25V, $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **SINGLE-ENDED INPUT ($\overline{PWRDWN}$)** | | | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | | | 2.0 | | 5.5 | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | -0.3 | | +0.8 | V |
| Input Current | $I_{IN}$ | $V_{IN}$ = high or low | | | -70 | | +70 | µA |
| Input Clamp Voltage | $V_{CL}$ | $I_{CL}$ = -18mA | | | | | -1.5 | V |
| **SINGLE-ENDED OUTPUTS (RxOUT_, RxCLK OUT)** | | | | | | | | |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -100µA | | | $V_{CCO}$ - 0.1 | | | V |
| | | $I_{OH}$ = -2mA | MAX9234/ MAX9236 | RxCLK OUT | $V_{CCO}$ - 0.25 | | | |
| | | | | RxOUT_ | $V_{CCO}$ - 0.40 | | | |
| | | | MAX9238 | | $V_{CCO}$ - 0.25 | | | |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 100µA | | | | | 0.1 | V |
| | | $I_{OL}$ = 2mA | MAX9234/ MAX9236 | RxCLK OUT | | | 0.2 | |
| | | | | RxOUT_ | | | 0.26 | |
| | | | MAX9238 | | | | 0.2 | |
| High-Impedance Output Current | $I_{OZ}$ | $\overline{PWRDWN}$ = low, $V_{OUT\_}$ = -0.3V to $V_{CCO}$ + 0.3V | | | -20 | | +20 | µA |
| Output Short-Circuit Current **(Note: Short one output at a time.)** | $I_{OS}$ | $V_{CCO}$ = 3.0V to 3.6V, $V_{OUT}$ = 0 | MAX9234/ MAX9236 | RxCLK OUT | -10 | | -40 | mA |
| | | | | RxOUT_ | -5 | | -20 | |
| | | | MAX9238 | | -10 | | -40 | |
| | | $V_{CCO}$ = 4.5V to 5.5V, $V_{OUT}$ = 0 | MAX9234/ MAX9236 | RxCLK OUT | -28 | | -75 | |
| | | | | RxOUT_ | -14 | | -37 | |
| | | | MAX9238 | | -28 | | -75 | |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +3.0V to +3.6V, $V_{CCO}$ = +3.0V to +5.5V, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = $V_{CCO}$ = +3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.25V, $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **LVDS INPUTS** | | | | | | | | |
| Differential Input-High Threshold | $V_{TH}$ | | | | | | 50 | mV |
| Differential Input-Low Threshold | $V_{TL}$ | | | | -50 | | | mV |
| Input Current | $I_{IN+}$, $I_{IN-}$ | $\overline{PWRDWN}$ = high or low | | | -25 | | +25 | µA |
| Power-Off Input Current | $I_{INO+}$, $I_{INO-}$ | $V_{CC}$ = $V_{CCO}$ = 0 or open, $\overline{PWRDWN}$ = 0 or open | | | -40 | | +40 | µA |
| Input Resistor 1 | $R_{IN1}$ | $\overline{PWRDWN}$ = high or low (Figure 1) | | | 42 | | 78 | kΩ |
| | | $V_{CC}$ = $V_{CCO}$ = 0 or open (Figure 1) | | | | | | |
| **POWER SUPPLY** | | | | | | | | |
| Worst-Case Supply Current | $I_{CCW}$ | $C_L$ = 8pF, worst-case pattern; $V_{CC}$ = $V_{CCO}$ = 3.0V to 3.6V, Figure 2 | MAX9234/ MAX9236 | 8MHz | | | 42 | mA |
| | | | | 16MHz | | | 57 | |
| | | | | 34MHz | | | 98 | |
| | | | MAX9238 | 16MHz | | | 63 | |
| | | | | 34MHz | | | 106 | |
| | | | | 66MHz | | | 177 | |
| Power-Down Supply Current | $I_{CCZ}$ | $\overline{PWRDWN}$ = low | | | | | 50 | µA |

# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = $V_{CCO}$ = +3.0V to +3.6V, 100m$V_{P-P}$ at 200kHz supply noise, $C_L$ = 8pF, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common mode voltage $V_{CM}$ = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = $V_{CCO}$ = +3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.25V, $T_A$ = +25°C.) (Notes 3, 4, 5)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Output Rise Time | CLHT | 0.1$V_{CCO}$ to 0.9$V_{CCO}$, Figure 3 | MAX9234/ MAX9236 | RxOUT | 3.52 | 5.04 | 6.24 | ns |
| | | | | RxCLK OUT | 2.2 | 3.15 | 3.9 | |
| | | | MAX9238 | | 2.2 | 3.15 | 3.9 | |
| Output Fall Time | CHLT | 0.9$V_{CCO}$ to 0.1$V_{CCO}$, Figure 3 | MAX9234/ MAX9236 | RxOUT | 1.95 | 3.18 | 4.35 | ns |
| | | | | RxCLK OUT | 1.3 | 2.12 | 2.9 | |
| | | | MAX9238 | | 1.3 | 2.12 | 2.9 | |
| RxIN Skew Margin | RSKM | Figure 4 (Note 6) | | 8MHz | 6600 | 7044 | | ps |
| | | | | 16MHz | 2560 | 3137 | | |
| | | | | 34MHz | 900 | 1327 | | |
| | | | MAX9238 | 66MHz | 330 | 685 | | |
| RxCLK OUT High Time | RCOH | Figures 5a, 5b | | | 0.35 x RCOP | | | ns |
| RxCLK OUT Low Time | RCOL | Figures 5a, 5b | | | 0.35 x RCOP | | | ns |
| RxOUT Setup to RxCLK OUT | RSRC | Figures 5a, 5b | | | 0.30 x RCOP | | | ns |
| RxOUT Hold from RxCLK OUT | RHRC | Figures 5a, 5b | | | 0.45 x RCOP | | | ns |
| RxCLK IN to RxCLK OUT Delay | RCCD | Figures 6a, 6b | | | 4.9 | 6.17 | 8.1 | ns |
| Deserializer Phase-Locked Loop Set | RPLLS | Figure 7 | | | | | 32800 x RCIP | ns |
| Deserializer Power-Down Delay | RPDD | Figure 8 | | | | | 100 | ns |

**Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except $V_{TH}$ and $V_{TL}$.

**Note 2:** Maximum and minimum limits overtemperature are guaranteed by design and characterization. Devices are production tested at $T_A$ = +25°C.

**Note 3:** AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ±6 sigma.

**Note 4:** $C_L$ includes probe and test jig capacitance.

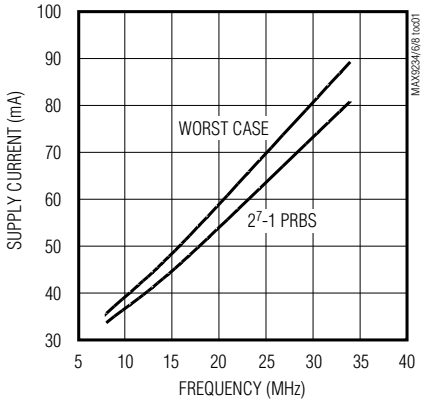
**Note 5:** RCIP is the period of RxCLK IN. RCOP is the period of RxCLK OUT. RCIP = RCOP.

**Note 6:** RSKM measured with ≤150ps cycle-to-cycle jitter on RxCLK IN.

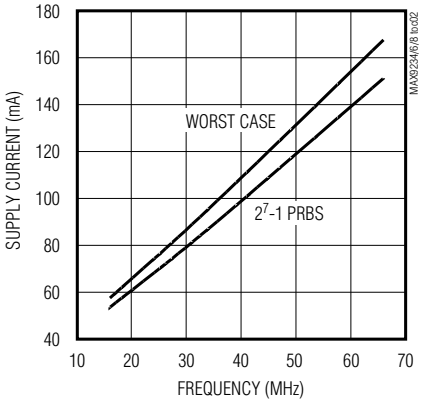
## Typical Operating Characteristics

($V_{CC}$ = $V_{CCO}$ = +3.3V, $C_L$ = 8pF, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.2V, input common-mode voltage $V_{CM}$ = 1.2V, $T_A$ = +25°C, unless otherwise noted.)

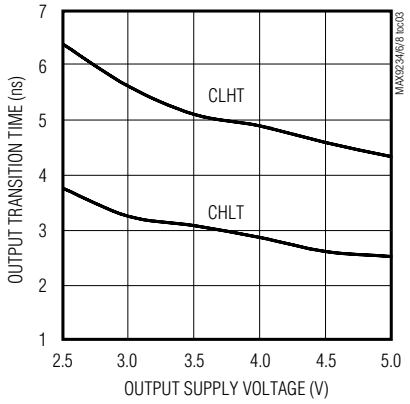
**MAX9234/MAX9236**
**WORST-CASE PATTERN AND PRBS**
**SUPPLY CURRENT vs. FREQUENCY**



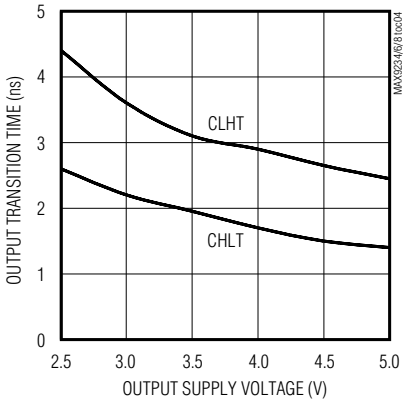

**MAX9238**
**WORST-CASE PATTERN AND PRBS**
**SUPPLY CURRENT vs. FREQUENCY**




**MAX9234/MAX9236**
**RxOUT TRANSITION TIME**
**vs. OUTPUT SUPPLY VOLTAGE ($V_{CCO}$)**




**MAX9238**
**RxOUT TRANSITION TIME**
**vs. OUTPUT SUPPLY VOLTAGE ($V_{CCO}$)**



# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 2, 4, 5, 45, 46, 47 | RxOUT14–RxOUT20 | Channel 2 Single-Ended Outputs |
| 3, 25, 32, 38, 44 | GND | Ground |
| 6 | N.C. | No Connect |
| 7, 13, 18 | LVDS GND | LVDS Ground |
| 8 | RxIN0- | Inverting Channel 0 LVDS Serial Data Input |
| 9 | RxIN0+ | Noninverting Channel 0 LVDS Serial Data Input |
| 10 | RxIN1- | Inverting Channel 1 LVDS Serial Data Input |
| 11 | RxIN1+ | Noninverting Channel 1 LVDS Serial Data Input |
| 12 | LVDS $V_{CC}$ | LVDS Supply Voltage. Bypass to LVDS GND with 0.1µF and 0.001µF capacitors in parallel as close to LVDS $V_{CC}$ as possible, with the smallest value capacitor closest to the supply pin. |
| 14 | RxIN2- | Inverting Channel 2 LVDS Serial Data Input |
| 15 | RxIN2+ | Noninverting Channel 2 LVDS Serial Data Input |
| 16 | RxCLK IN- | Inverting LVDS Parallel Rate Clock Input |
| 17 | RxCLK IN+ | Noninverting LVDS Parallel Rate Clock Input |
| 19, 21 | PLL GND | PLL Ground |
| 20 | PLL $V_{CC}$ | PLL Supply Voltage. Bypass to PLL GND with 0.1µF and 0.001µF capacitors in parallel as close to PLL $V_{CC}$ as possible, with the smallest value capacitor closest to the supply pin. |
| 22 | $\overline{PWRDWN}$ | 5V Tolerant LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND. Outputs are high impedance when $\overline{PWRDWN}$ = low or open. |
| 23 | RxCLK OUT | Parallel Rate Clock Single-Ended Output. The MAX9234 has a rising-edge strobe. The MAX9236/MAX9238 have a falling-edge strobe. |
| 24, 26, 27, 29, 30, 31, 33 | RxOUT0–RxOUT6 | Channel 0 Single-Ended Outputs |
| 28, 36, 48 | $V_{CCO}$ | Output Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to $V_{CCO}$ as possible, with the smallest value capacitor closest to the supply pin. |
| 34, 35, 37, 39, 40, 41, 43 | RxOUT7–RxOUT13 | Channel 1 Single-Ended Outputs |
| 42 | $V_{CC}$ | Digital Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to $V_{CC}$ as possible, with the smallest value capacitor closest to the supply pin. |

**Table 1. Part Equivalent Table**

| PART | EQUIVALENT WITH DCB/NC = HIGH OR OPEN | OPERATING FREQUENCY (MHz) | OUTPUT STROBE |
|---|---|---|---|
| MAX9234 | MAX9210 | 8 to 34 | Rising edge |
| MAX9236 | MAX9220 | 8 to 34 | Falling edge |
| MAX9238 | MAX9222 | 16 to 66 | Falling edge |

## Detailed Description

The MAX9234/MAX9236 operate at a parallel clock frequency of 8MHz to 34MHz. The MAX9238 operates at a parallel clock frequency of 16MHz to 66MHz. The transition times of the single-ended outputs are increased on the MAX9234/MAX9236 for reduced EMI.

### DC Balance

Data coding by the MAX9209/MAX9211/MAX9213/MAX9215 serializers (which are companion devices to the MAX9234/MAX9236/MAX9238 deserializers) limits the imbalance of ones and zeros transmitted on each channel. If +1 is assigned to each binary 1 transmitted and -1 is assigned to each binary 0 transmitted, the variation in the running sum of assigned values is called the digital sum variation (DSV). The maximum DSV for the data channels is 10. At most, 10 more zeros than ones, or 10 more ones than zeros, are transmitted. The maximum DSV for the clock channel is five. Limiting the DSV and choosing the correct coupling capacitors maintains differential signal amplitude and reduces jitter due to droop on AC-coupled links.

To obtain DC balance on the data channels, the serializer parallel data is inverted or not inverted, depending on the sign of the digital sum at the word boundary. Two complementary bits are appended to each group of 7 parallel input data bits to indicate to the MAX9234/MAX9236/MAX9238 deserializers whether the data bits are inverted (see Figure 9). The deserializer restores the original state of the parallel data. The LVDS clock signal alternates duty cycles of 4/9 and 5/9, which maintain DC balance.

### AC-Coupling Benefits

Bit errors experienced with DC-coupling can be eliminated by increasing the receiver common-mode voltage range by AC-coupling. AC-coupling increases the common-mode voltage range of an LVDS receiver to nearly the voltage rating of the capacitor. The typical LVDS driver output is 350mV centered on an offset voltage of 1.25V, making single-ended output voltages of 1.425V and 1.075V. An LVDS receiver accepts signals from 0 to 2.4V, allowing approximately ±1V common-mode difference between the driver and receiver on a DC-coupled link (2.4V - 1.425V = 0.975V and 1.075V - 0V = 1.075V). Common-mode voltage differences may be due to ground potential variation or common-mode noise. If there is more than ±1V of difference, the receiver is not guaranteed to read the input signal correctly and may cause bit errors. AC-coupling filters low-frequency ground shifts and common-mode noise and passes high-frequency data. A common-mode voltage difference up to the voltage rating of the coupling capacitor (minus half the differential swing) is tolerated. DC-balanced coding of the data is required to maintain the differential signal amplitude and limit jitter on an AC-coupled link. A capacitor in series with each output of the LVDS driver is sufficient for AC-coupling. However, two capacitors—one at the serializer output and one at the deserializer input—provide protection in case either end of the cable is shorted to a high voltage.

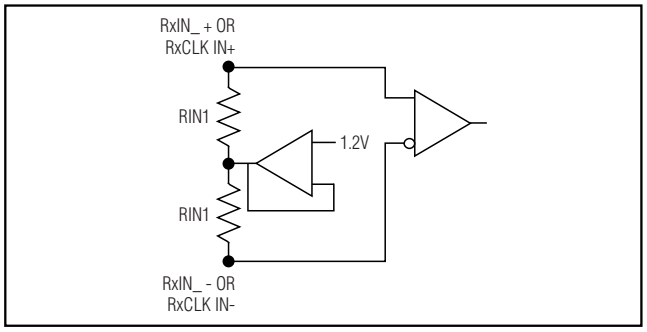



*Figure 1. LVDS Input Circuit*

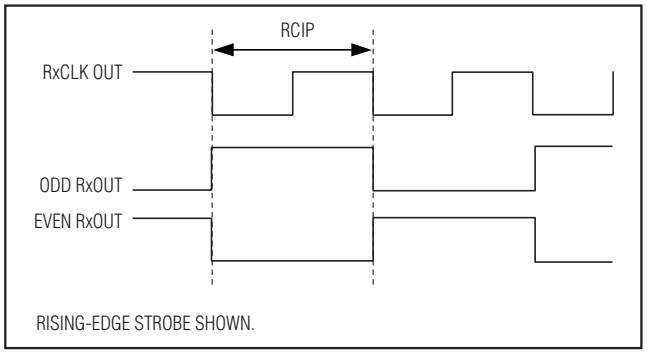



*Figure 2. Worst-Case Test Pattern*

# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers

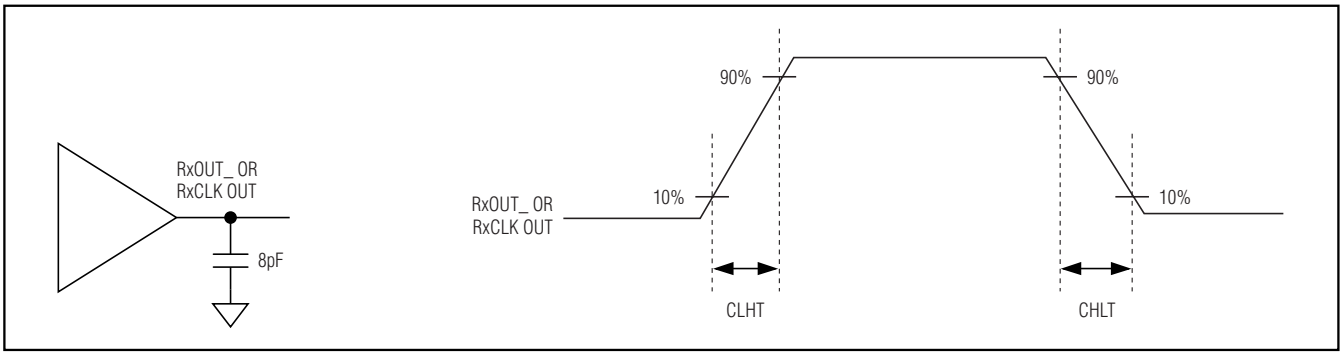



*Figure 3. Output Load and Transition Times*

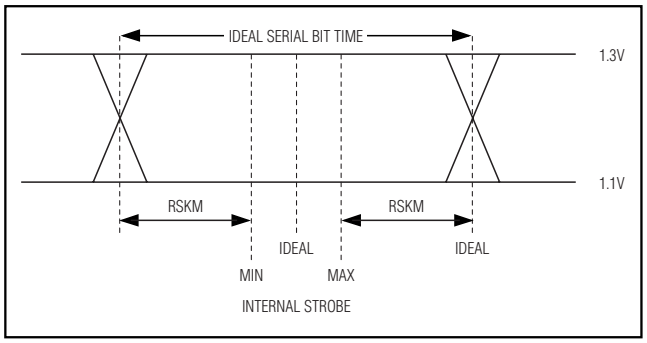



*Figure 4. LVDS Receiver Input Skew Margin*

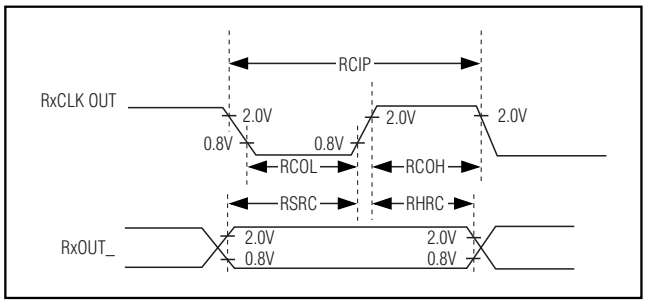



*Figure 5a. MAX9234 Output Setup/Hold and High/Low Times*

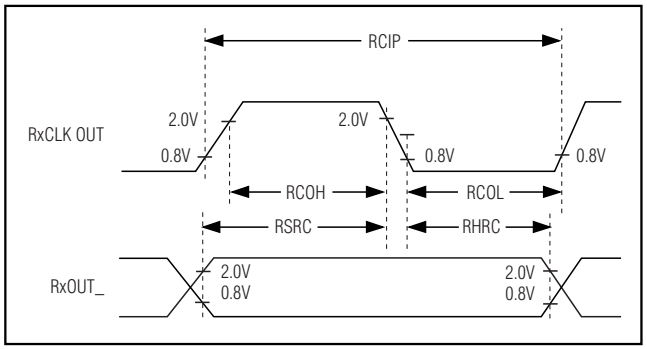



*Figure 5b. MAX9236/MAX9238 Output Setup/Hold and High/Low Times*

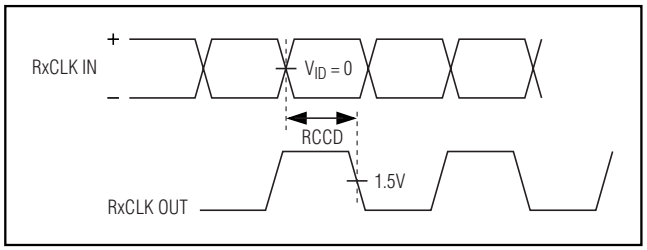



*Figure 6a. MAX9234 Clock-IN to Clock-OUT Delay*

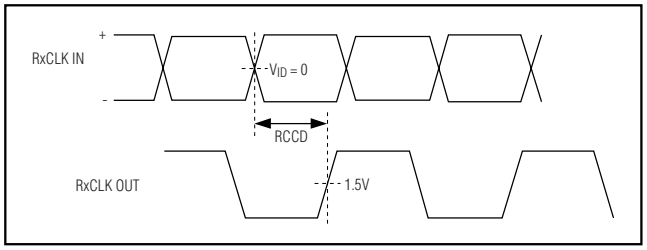



*Figure 6b. MAX9236/MAX9238 Clock-IN to Clock-OUT Delay*

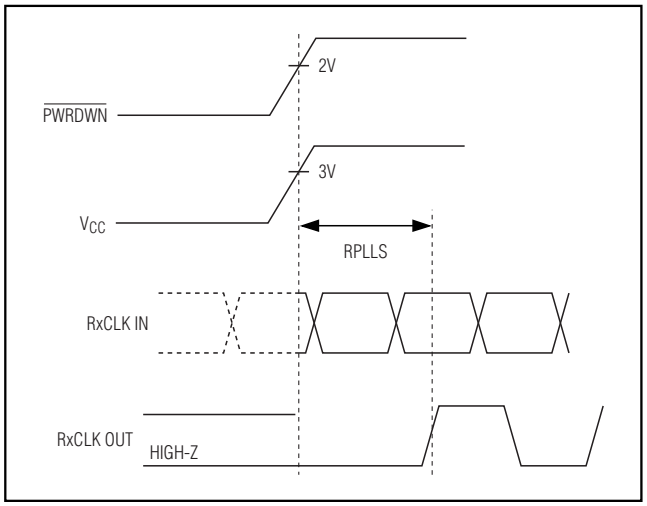



*Figure 7. Phase-Locked Loop Set Time*

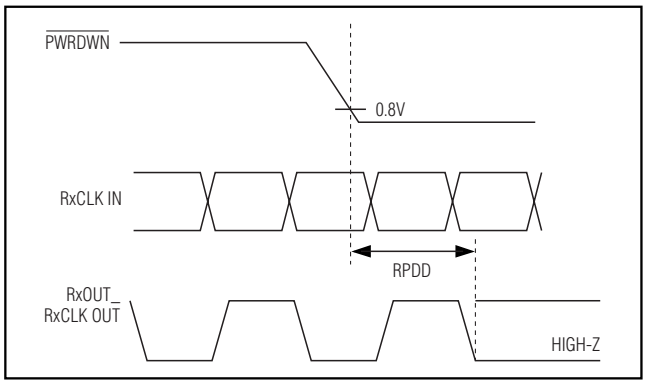



*Figure 8. Power-Down Delay*

### MAX9234/MAX9236/MAX9238 vs. MAX9210/MAX9220/MAX9222

The MAX9234/MAX9236/MAX9238 operate in DC-balance mode only. Pinouts are the same as the MAX9210/MAX9220/MAX9222 except that pin 6 on the MAX9234/MAX9236/MAX9238 is no connect (N.C.). DC balance allows AC-coupling with series capacitors. The MAX9234/MAX9236/MAX9238 are hot-swappable and the input frequency can be changed on the fly, but otherwise the specifications and functionality are the same as the MAX9210/MAX9220/MAX9222 operating in DC-balance mode. See Table 1.

## Applications Information

### Selection of AC-Coupling Capacitors

Voltage droop and the DSV of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level.

The RC network for an AC-coupled link consists of the LVDS receiver termination resistor ($R_T$), the LVDS driver output resistor ($R_O$), and the series AC-coupling capacitors (C). The RC time constant for two equal-value series capacitors is (C x ($R_T$ + $R_O$)) / 2 (Figure 10). The RC time constant for four equal-value series capacitors is (C x ($R_T$ + $R_O$)) / 4 (Figure 11).

$R_T$ is required to match the transmission line impedance (usually 100Ω) and $R_O$ is determined by the LVDS driver design (the minimum differential output resistance of 78Ω for the MAX9209/MAX9211/MAX9213/MAX9215 serializers is used in the following example). This leaves the capacitor selection to change the system time constant.

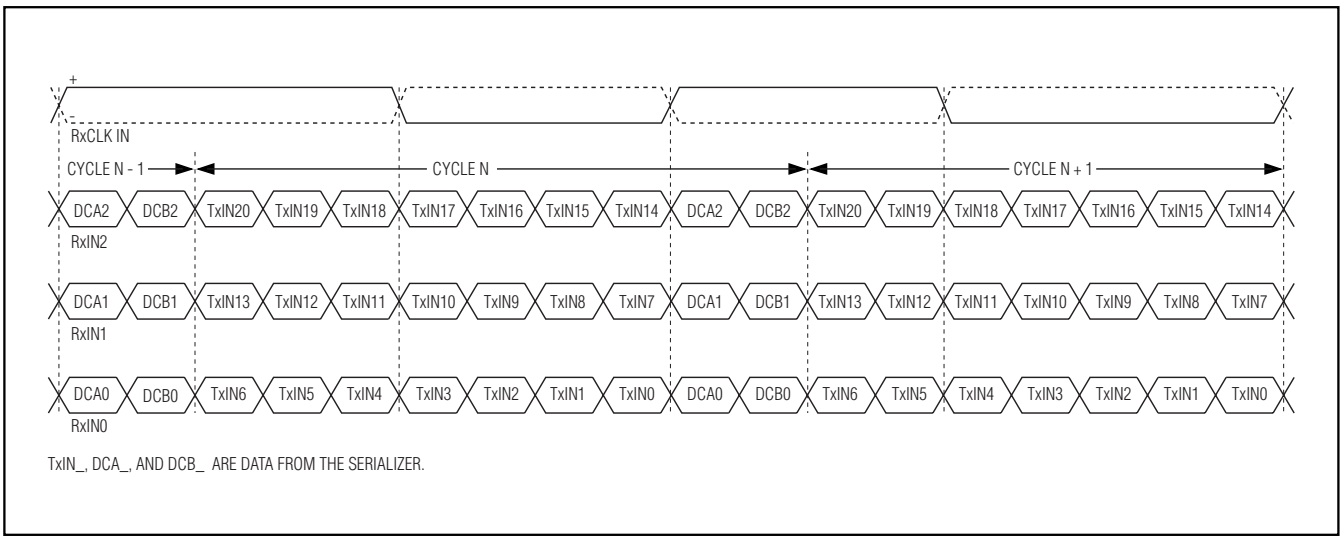



*Figure 9. Deserializer Serial Input*

# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers

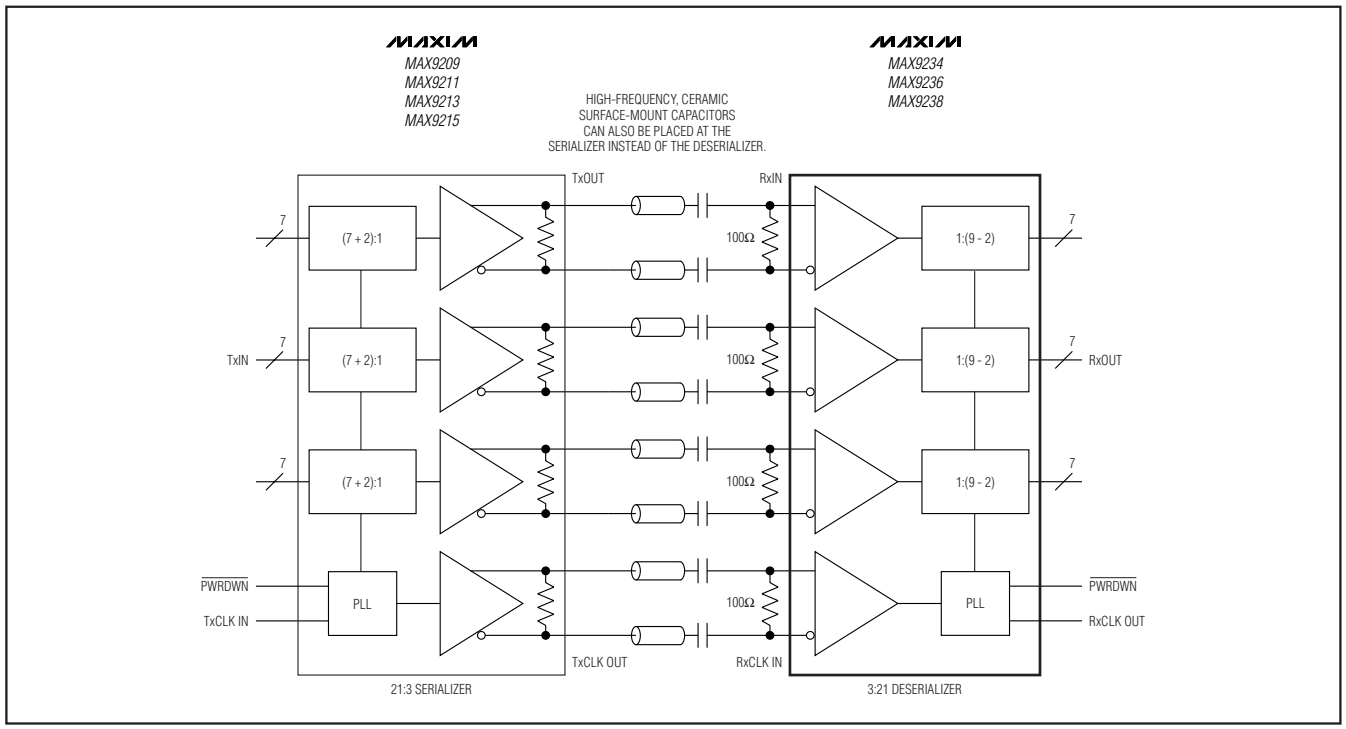



*Figure 10. Two Capacitors per Link, AC-Coupled*

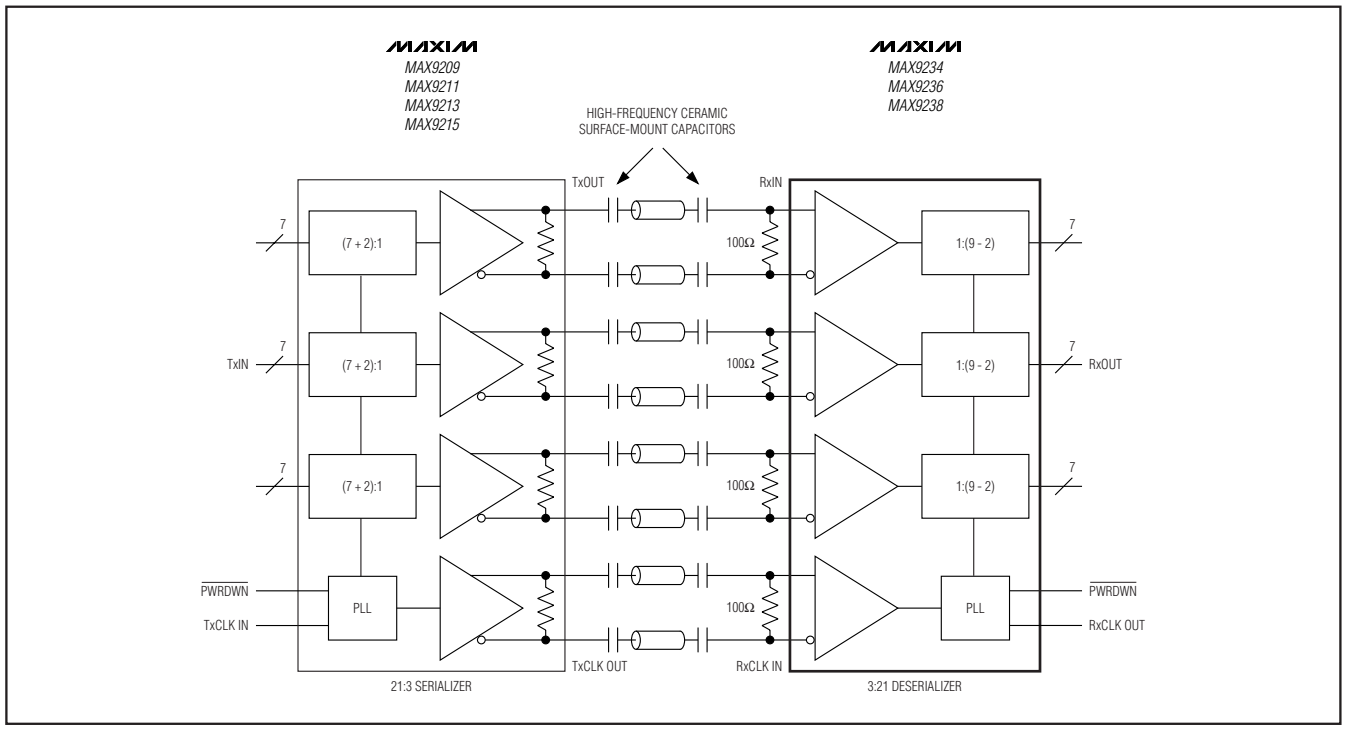



*Figure 11. Four Capacitors per Link, AC-Coupled*

In the following example, the capacitor value for a droop of 2% is calculated. Jitter due to this droop is then calculated assuming a 1ns transition time:

$$C = - (2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \quad \text{(Eq 1)}$$

where:
C = AC-coupling capacitor (F).
$t_B$ = bit time (s).
DSV = digital sum variation (integer).
ln = natural log.
D = droop (% of signal amplitude).
$R_T$ = termination resistor (Ω).
$R_O$ = output resistance (Ω).

Equation 1 is for two series capacitors (Figure 10). The bit time ($t_B$) is the period of the parallel clock divided by 9. The DSV is 10. See equation 3 for four series capacitors (Figure 11).

The capacitor for 2% maximum droop at 8MHz parallel rate clock is:

$$C = - (2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O))$$

$$C = - (2 \times 13.9ns \times 10) / (\ln (1 - 0.02) \times (100\Omega + 78\Omega))$$

$$C = 0.0773\mu F$$

Jitter due to droop is proportional to the droop and transition time:

$$t_J = t_T \times D \quad \text{(Eq 2)}$$

where:
$t_J$ = jitter (s).
$t_T$ = transition time (s) (0 to 100%).
D = droop (% of signal amplitude).

Jitter due to 2% droop and assumed 1ns transition time is:

$$t_J = 1ns \times 0.02$$

$$t_J = 20ps$$

The transition time in a real system depends on the frequency response of the cable driven by the serializer. The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Equation 1 altered for four series capacitors (Figure 11) is:

$$C = - (4 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \quad \text{(Eq 3)}$$

### Input Bias and Frequency Detection

The inverting and noninverting LVDS inputs are internally connected to +1.2V through 42kΩ (min) to provide biasing for AC-coupling (Figure 1). A frequency-detection circuit on the clock input detects when the input is not switching, or is switching at low frequency. In this case, all outputs are driven low. To prevent switching due to noise when the clock input is not driven, bias the clock input to differential +15mV by connecting a 10kΩ ±1% pullup resistor between the noninverting input and $V_{CC}$, and a 10kΩ ±1% pulldown resistor between the inverting input and ground. These bias resistors, along with the 100Ω ±1% tolerance termination resistor, provide +15mV of differential input.

### Unused LVDS Data Inputs

At each unused LVDS data input, pull the inverting input up to $V_{CC}$ using a 10kΩ resistor, and pull the noninverting input down to ground using a 10kΩ resistor. Do not connect a termination resistor. The pullup and pulldown resistors drive the corresponding outputs low and prevent switching due to noise.

### $\overline{PWRDWN}$

Driving $\overline{PWRDWN}$ low puts the outputs in high impedance, stops the PLL, and reduces supply current to 50µA or less. Driving $\overline{PWRDWN}$ high drives the outputs low until the PLL locks. The outputs of two deserializers can be bused to form a 2:1 mux with the outputs controlled by $\overline{PWRDWN}$. Wait 100ns between disabling one deserializer (driving $\overline{PWRDWN}$ low) and enabling the second one (driving $\overline{PWRDWN}$ high) to avoid contention of the bused outputs.

### Input Clock and PLL Lock Time

There is no required timing sequence for the application or reapplication of the parallel rate clock (RxCLK IN) relative to $\overline{PWRDWN}$, or to a power-supply ramp for proper PLL lock. The PLL lock time is set by an internal counter. The maximum time to lock is 32,800 clock periods. Power and clock should be stable to meet the lock-time specification. When the PLL is locking, the outputs are low.

# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers

### Power-Supply Bypassing

There are separate on-chip power domains for digital circuits, outputs, PLL, and LVDS inputs. Bypass each $V_{CC}$, $V_{CCO}$, PLL $V_{CC}$, and LVDS $V_{CC}$ pin with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

### Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

### Board Layout

Keep the LVTTL/LVCMOS outputs and LVDS input signals separated to prevent crosstalk. A four-layer PC board with separate layers for power, ground, LVDS inputs, and digital signals is recommended.

### ESD Protection

The MAX9234/MAX9236/MAX9238 ESD tolerance is rated for Human Body Model and ISO 10605 standards. ISO 10605 specifies ESD tolerance for electronic systems. The Human Body Model discharge components are $C_S$ = 100pF and $R_D$ = 1.5kΩ (Figure 12). For the Human Body Model, all pins are rated for ±5kV contact discharge. The ISO 10605 discharge components are $C_S$ = 330pF and $R_D$ = 2kΩ (Figure 13). For ISO 10605, the LVDS outputs are rated for ±8kV contact and ±25kV air discharge.

### 5V Tolerant Input

$\overline{PWRDWN}$ is 5V tolerant and is internally pulled down to GND.

### Skew Margin (RSKM)

Skew margin (RSKM) is the time allowed for degradation of the serial data sampling setup and hold times by sources other than the deserializer. The deserializer sampling uncertainty is accounted for and does not need to be subtracted from RSKM. The main outside contributors of jitter and skew that subtract from RSKM are interconnect intersymbol interference, serializer pulse position uncertainty, and pair-to-pair path skew.

### $V_{CCO}$ Output Supply and Power Dissipation

The outputs have a separate supply ($V_{CCO}$) for interfacing to systems with 1.8V to 5V nominal input-logic levels. The *DC Electrical Characteristics* table gives the maximum supply current for $V_{CCO}$ = 3.6V with 8pF load at several switching frequencies with all outputs switching in the worst-case switching pattern. The approximate incremental supply current for $V_{CCO}$ other than 3.6V with the same 8pF load and worst-case pattern can be calculated using:

$$I_I = C_T V_I\, 0.5 f_C \times 21 \text{ (data outputs)} + C_T V_I f_C \times 1 \text{ (clock output)}$$

where:
$I_I$ = incremental supply current.
$C_T$ = total internal ($C_{INT}$) and external ($C_L$) load capacitance.
$V_I$ = incremental supply voltage.
$f_C$ = output clock-switching frequency.

The incremental current is added to (for $V_{CCO}$ > 3.6V) or subtracted from (for $V_{CCO}$ < 3.6V) the *DC Electrical Characteristics* table maximum supply current. The internal output buffer capacitance is $C_{INT}$ = 6pF. The worst-case pattern-switching frequency of the data outputs is half the switching frequency of the output clock.

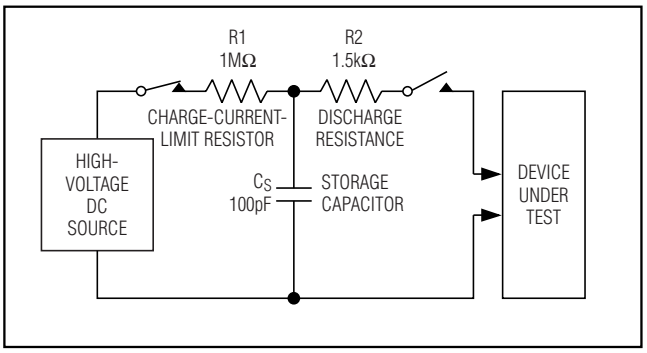



*Figure 12. Human Body ESD Test Circuit*

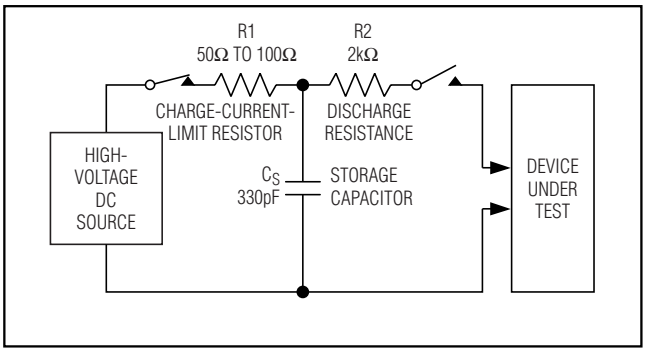



*Figure 13. ISO 10605 Contact Discharge ESD Test Circuit*

In the following example, the incremental supply current is calculated for $V_{CCO}$ = 5.5V, $f_C$ = 34MHz, and $C_L$ = 8pF:

$$V_I = 5.5V - 3.6V = 1.9V$$

$$C_T = C_{INT} + C_L = 6pF + 8pF = 14pF$$

where:

$I_I = C_T V_I\, 0.5 f_C$ x 21 (data outputs) + $C_T V_I f_C$ x 1 (clock output).

$I_I$ = (14pF x 1.9V x 0.5 x 34MHz x 21) + (14pF x 1.9V x 34MHz).

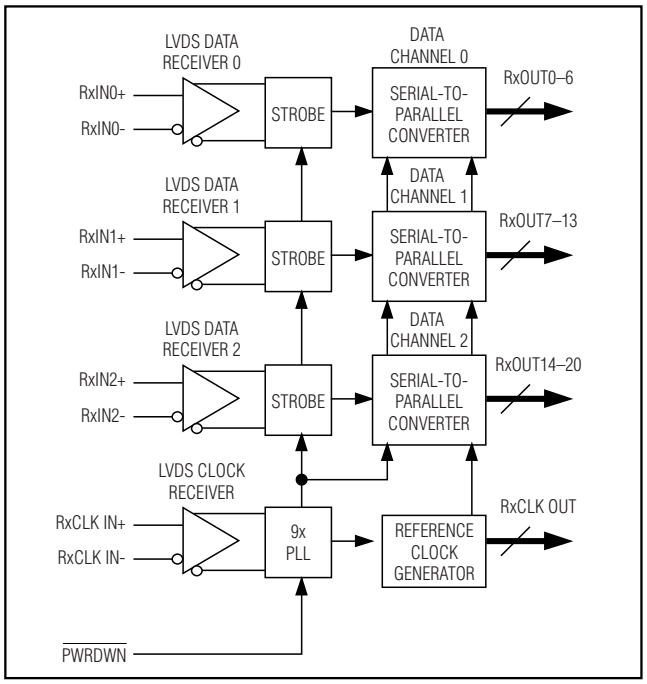
$I_I$ = 9.5mA + 0.9mA = 10.4mA.

The maximum supply current in DC-balanced mode for $V_{CC}$ = $V_{CCO}$ = 3.6V at $f_C$ = 34MHz is 106mA (from the *DC Electrical Characteristics* table). Add 10.4mA to get the total approximate maximum supply current at $V_{CCO}$ = 5.5V and $V_{CC}$ = 3.6V.

If the output supply voltage is less than $V_{CCO}$ = 3.6V, the reduced supply current can be calculated using the same formula and method.

At high switching frequency, high supply voltage, and high capacitive loading, power dissipation can exceed the package power-dissipation rating. Do not exceed the maximum package power-dissipation rating. See the *Absolute Maximum Ratings* for maximum package power-dissipation capacity and temperature derating.

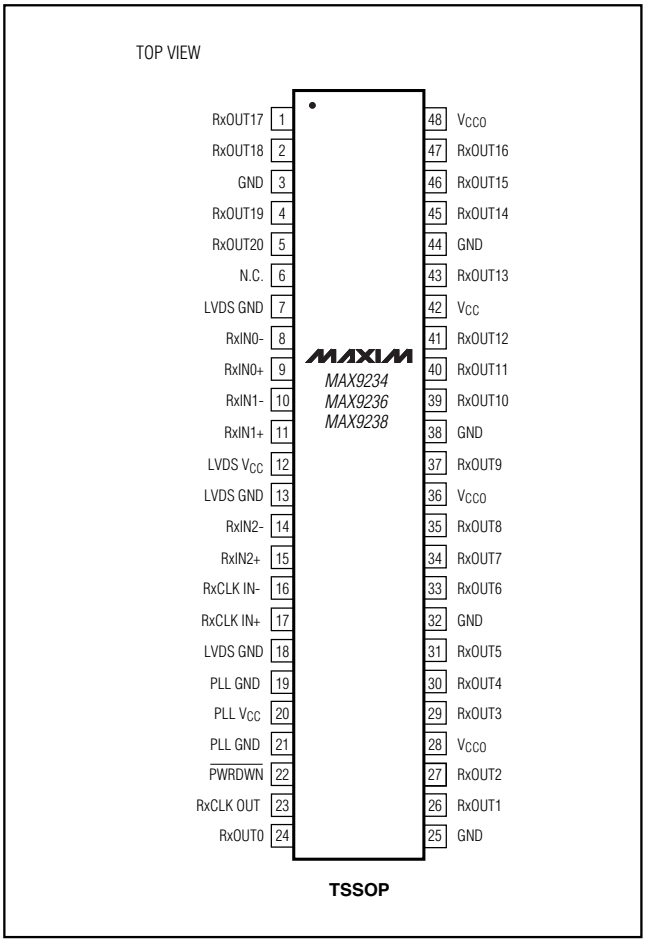
## Functional Diagram




### Rising- or Falling-Edge Output Strobe

The MAX9234 has a rising-edge output strobe, which latches the parallel output data into the next chip on the rising edge of RxCLK OUT. The MAX9236/MAX9238 have a falling-edge output strobe, which latches the parallel output data into the next chip on the falling edge of RxCLK OUT. The deserializer output strobe polarity does not need to match the serializer input strobe polarity. A deserializer with rising- or falling-edge output strobe can be driven by a serializer with a rising-edge input strobe.

## Pin Configuration




## Chip Information

MAX9234 TRANSISTOR COUNT: 14,104

MAX9236 TRANSISTOR COUNT: 14,104

MAX9238 TRANSISTOR COUNT: 14,104

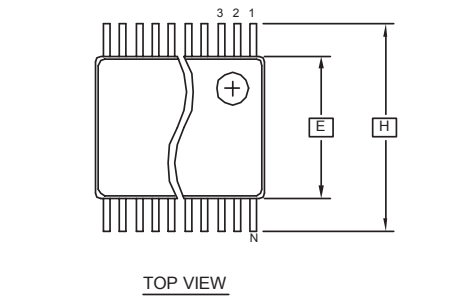
PROCESS: CMOS

# Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers

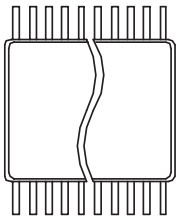
## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

48L TSSOP.EPS

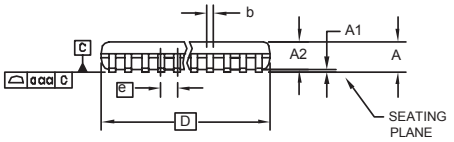



TOP VIEW

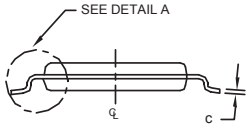


BOTTOM VIEW

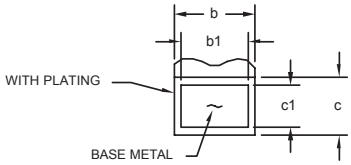
| SYMBOL | COMMON DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | -- | -- | 1.10 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 0.55 | 0.90 | 0.95 |
| aaa | | 0.10 | |
| b | 0.17 | -- | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.09 | -- | 0.20 |
| c1 | 0.09 | 0.127 | 0.16 |
| D | 12.40 | 12.50 | 12.60 |
| E | 6.00 | 6.10 | 6.20 |
| e | | 0.50 BSC | |
| H | | 8.10 BSC | |
| L | 0.50 | 0.60 | 0.75 |
| N | | 48 | |
| ; | 0° | -- | 8° |



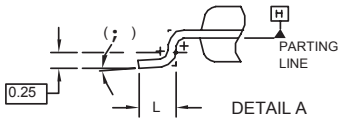

SIDE VIEW




END VIEW




SECTION C-C




DETAIL A

NOTES:

1. DIMENSIONS D & E ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM ON D SIDE, AND 0.25MM ON E SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153, VARIATIONS, ED.
5. "N" REFERS TO NUMBER OF LEADS.
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM (-C-), THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM (-C-) IN THE DIRECTION INDICATED.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 48L TSSOP, 6.1mm BODY

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0155 | B | 1/1 |

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